AMENDMENTS TO THE CLAIMS

Please cancel Claims 1-10, without prejudice.

1-10. (Cancelled)

11. (Previously presented) A digital apparatus for simulating signals of a simulated system, said system being simulated comprising subsystems and connections between said subsystems, said signals being referred to said connections, said apparatus comprising:

means for entering a representation of said system;

means for transforming said representation into a computational graph, said computation graph comprising at least one of computation nodes, each computation node having a computation rule;

a scheduler for scheduling the execution of said computation rules of said computation nodes in time, said scheduler being adapted for scheduling the execution of said computation rule for each computation node such that for a maximum amount of computation nodes at least a sequence of computations can be performed without interruptions;

means for execution said computation rules in the order determined by said scheduler.

12. (Previously presented) The apparatus recited in Claim 11, wherein the apparatus is further adapted such that at least one of said signals is represented by a sum of at least two carriers, each carrier being modulated by a bandpass signal, wherein at least two of said bandpass signals have a different bandwidth.

13. (Previously presented) The apparatus recited in Claim11, wherein the apparatus is further adapted such that at least two of said signals are represented by a sum of at least two carriers, each carrier being modulated by a bandpass signal, wherein at least two of said signals have a representation being different from signal to signal in either at least one carrier frequency or in at least one bandwidth for a carrier frequency common for said two signals.

14. (Previously presented) The apparatus recited in Claim 11, wherein the transforming means comprises:

means for adding decimators and interpolators;

means for splitting a node relating to a linear subcircuit into a plurality of nodes; and

means for selecting an appropriate computation method for nonlinear circuits.

15. (Previously presented) The apparatus recited in Claim 11, wherein the computation nodes

comprise a plurality of nodes each having a different level of priority, and wherein the scheduler is configured to schedule the execution for the node having the highest level of priority.

16. (Previously presented) The apparatus recited in Claim 15, wherein the plurality of computation nodes comprise:

a first node which is not ready for execution;

a second node which is not in a feedback loop and ready for sample-by-sample execution;

a third node which is in a feedback loop and ready for sample-by-sample execution; and

a fourth node which is ready for vector processing.

17. (Previously presented) A digital apparatus for simulating signals in a simulated system, the apparatus comprising:

an entering section configured to enter a representation of said system;

a transforming section configured to transform the representation into a computational graph, the computation graph comprising a plurality of computation nodes, each computation node having a computation rule;

a scheduler configured to schedule the execution of the computation rules of the computation nodes in time, the scheduler being adapted to schedule the execution of the computation rule for each computation node such that for a maximum amount of computation nodes at least a sequence of computations can be performed without interruptions; and

an execution section configured to execute the computation rules in the order determined by the scheduler.